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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/919,283
Filing Date: July 31, 2001
Appellant(s): GALBI ET AL.

Steven L. Webb
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/28/2005 appealing from the Office action mailed 8/3/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,724,767	Chong et al	04-2004
6,021,132	Muller et al	02-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims **1, 3, 5-6, 10-11, 13, 15-16, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,724,767 to Chong et al in view of U.S. Patent Number 6,021,132 to Muller et al.

Regarding claim **1**, Chong discloses a core processor (the RISC microcontroller 240 of Figure 3) configured to execute software to process a series of communication packets (see line 64 of column 6 through line 1 of column 7), the processing of each packet being an event and having associated data and context information; and a co-processor (processing engine 10 in Figures 1-3) comprising a plurality of state information buffers (queue descriptor 500 of Figure 6, for example) for storing state information, a plurality of context buffers (buffer descriptors – element 570 for example) for storing context information associated with a plurality of events and a plurality of data buffers (packet descriptors – element 560 for example) for storing data associated with the plurality of events where the state information comprises a data buffer pointer (NP 320 of Chong) pointing to one of the plurality of data buffers and a context buffer pointer (NB 330 of Chong) pointing to one of the plurality of context buffers.

Regarding claims **10, 11, and 16**, Chong discloses the analogous limitations of those claims as discussed regarding claim 1 above.

Chong does not disclose expressly the limitation of using an in-use counter in the state buffers (claim 1, 10, 11, and 16) or in the context and data buffers (claims 10 and 16). Chong also does not disclose the limitation of claims 10 and 16 of transferring data between events by changing the data in the state information buffer.

However, Muller discloses the concept of buffer ownership throughout, indicating that this is necessary in the shared memory management scheme discussed therein. For example,

lines 37-40 of column 6 and lines 34-36 of column 11 discuss the need for tracking the number of owners of a given buffer in order to know when the buffer can properly be released in a shared memory scheme. Muller also discusses the transfer of buffer ownership by updating the count field from line 16 of column 11 through line 37 of column 12. In a combination of Muller with Chong, it is clear that (as indicated in Muller in lines 37-40 of column 6 and lines 34-36 of column 11) buffer ownership would be tracked using ownership counts which are analogous to the in-use counts of the present invention. Further, it would be necessary at times to transfer ownership of these shared buffers (as described in Muller in columns 11 and 12) by changing a state variable (the ownership count). Muller further discloses the limitations of claim 11 of incrementing the in-use counter associated with said state information buffer when an event is associated with said state information buffer (lines 34-36 of column 11 and line 61 of column 11 through line 2 of column 12); and decrementing the in-use counter of said state information buffer when said event associated with said buffer is finished (lines 22-29 of column 7 and lines 49-53 of column 12). Chong and Muller are analogous art because they are from the same field of endeavor of high-speed packet switching.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the shared memory management scheme of Muller with Chong. Specifically, it would have been obvious to use a shared memory scheme like that of Muller to share common memory resources dynamically among all input/output ports and thus to more efficiently manage the memory resources (see lines 1-18 of column 2 of Muller).

The motivation for doing so would have been to provide more efficient use of memory resources in a switching system as discussed in lines 1-10 of column 2. Therefore, it would have

been obvious to combine Muller with Chong for the benefit of better use of memory resources to obtain the invention as specified in claims 1, 10, 11, and 16.

Regarding claims **3 and 5**, as indicated above regarding claims 10 and 16, Muller discloses the limitation of an in-use counter for buffers in a shared memory scheme throughout and specifically in lines 37-40 of column 6 and lines 34-36 of column 11. Thus, as indicated above, Chong, modified by Muller as above, discloses the limitations of claims 3 and 5 of an in-use counter associated with the context buffers and the data buffers.

Similarly, regarding claim **6**, as indicated above regarding claims 10 and 16, Muller discloses the limitation of transferring data between events by changing in a data buffer in the discussion of buffer ownership transfer processing in columns 11 and 12. Thus, as indicated above, Chong, modified by Muller as above, discloses the limitations of claim 6 of transferring data from one event to another.

Regarding claims **13, 15, and 20**, Chong doesn't disclose expressly the limitation of incrementing and decrementing an in-use counter when events are associated with the context or data buffers. Muller discloses incrementing the in-use counter associated with said context (data) buffer when an event is associated with said context (data) buffer (lines 34-36 of column 11 and line 61 of column 11 through line 2 of column 12); and decrementing the in-use counter of said context (data) buffer when said event associated with said context (data) buffer is finished (lines 22-29 of column 7 and lines 49-53 of column 12).

Chong and Muller are analogous art because they are from the same field of endeavor of high-speed packet switching.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the shared memory management scheme of Muller with Chong. Specifically, it would have been obvious to use a shared memory scheme like that of Muller to share common memory resources dynamically among all input/output ports and thus to more efficiently manage the memory resources (see lines 1-18 of column 2 of Muller).

The motivation for doing so would have been to provide more efficient use of memory resources in a switching system as discussed in lines 1-10 of column 2. Therefore, it would have been obvious to combine Muller with Chong for the benefit of better use of memory resources to obtain the invention as specified in claims 13, 15 and 20.

(10) Response to Argument

The arguments regarding the art rejections in the section titled "Argument" on pages 6-10 are not persuasive for the following reasons:

In subsection I of the Argument section, Applicant summarizes the arguments regarding the rejection of claims 1, 3, 5, 6, 10, 11, 13, 15, 16, and 20 under 35 U.S.C. 103(a).

In subsection II of the Argument section, Applicant cites various sections of the MPEP and case law regarding the requirements for a prima facie obviousness rejection. Examiner believes the rejections to be valid as discussed below.

In subsection III of the Argument section, Applicant addresses the rejection of claims 1, 3, 5, and 6 under 35 U.S.C. 103(a). In the first paragraph of this subsection, Applicant includes information from claim 1. Applicant also includes other material related to claim 1, but not

specified in the claims. For example, Applicant states that the buffers are on-chip hardware buffers. Applicant also discusses the size of the buffers and other properties which are not specifically claimed.

In the second paragraph of subsection III, Applicant argues that Chong does not disclose a plurality of state information buffers, context buffers, or data buffers formed as part of a co-processor. Examiner respectfully disagrees. As stated explicitly in the Final Office Action and in section (9) above, Chong has disclosed these buffers in elements 500, 570, and 560 of Figure 6, respectively. Applicant then argues that Chong forms a data structure comprising a two dimensional linked list. While this may be true, it does not change the fact that elements 500, 570, and 560 of Figure 6 of Chong disclose the three buffers as recited in the claims. Applicant argues that the buffers in Chong are part of the data structure and thus not part of the co-processor. Applicant states that the data structure is created dynamically for each VC and stored in the general internal memory of the chip. However, as discussed in the rejection, processing engine 10 is the co-processor of Chong. Internal memory 80 is part of this element (see Figure 1, for example) and thus, the buffers stored in this memory are in fact part of the co-processor, regardless of when they are created. Applicant has conceded that this is the case and this is also supported by Chong; for example, see lines 32-33 of column 6 ("the data structure is preferably queued in internal memory").

In summary, the difference between the Applicant's view and the Examiner's view is largely as follows. The Applicant believes that the claim language requires hardware buffers like those disclosed in portions of the specification while the Examiner believes that the claim

language reads on software buffers which are part of the internal memory of a co-processor like those in Chong.

In the third paragraph of this subsection, Applicant states that Muller does not teach a co-processor having state buffers, data buffers, and context buffers. However, the rejection relied upon Chong for this teaching as discussed above.

In the fourth and fifth paragraphs of subsection III, Applicant reasserts the argument that claim 1 as well as dependent claims 3, 5, and 6 are allowable. For reasons stated above, Examiner respectfully disagrees and believes the rejection to be valid.

In subsection IV of the Argument section, in regard to claim 10, Applicant largely restates the previous argument that Chong does not teach a co-processor having a plurality of state information buffers, a plurality of context buffers and a plurality of data buffers. Examiner respectfully disagrees for reasons stated above and believes the rejection of claim 10 to be valid.

In subsection V of the Argument section, in regard to claims 11, 13, and 15, Applicant largely restates the previous argument that Chong does not teach a co-processor having a plurality of state information buffers, a plurality of context buffers and a plurality of data buffers. Examiner respectfully disagrees for reasons stated above and believes the rejection of claims 11, 13, and 15 to be valid.

In subsection VI of the Argument section, in regard to claims 16 and 20, Applicant largely restates the previous argument that Chong does not teach a co-processor having a

plurality of state information buffers, a plurality of context buffers and a plurality of data buffers. Examiner respectfully disagrees for reasons stated above and believes the rejection of claims 16 and 20 to be valid.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Robert C Scheibel 12-5-05

Robert C. Scheibel, Jr.

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